Please amend the claims as follows:

CLAIM 8 (amended)

The method of claim 1 further including the steps of:

forming a P+ collector plug region in said N base region for said PNP transistor so that said P+ collector plug region is incorporated into said P+ collector for said PNP transistor;

forming an N+ collector plug region in said P intrinsic base region for said NPN transistor so that said N+ collector plug region is incorporated into said N collector region of said N+ sub-collector region for said NPN transistor;

forming individual conductive metal contacts with said collector plug regions; and

forming an oxide region between said collector plug metal contacts.

Please add the following new claims:

CLAIM 19

A method for fabricating complementary vertical PNP and NPN bipolar junction transistors, said method comprising:

forming said PNP and said NPN transistors on a single substrate, wherein forming said PNP and NPN transistors includes forming an N silicon layer to become an intrinsic base region for said PNP transistor and a collector region for said NPN transistor.

CLAIM 20